REMARKS

The Office Action dated June 29, 2004, has been received and carefully considered. In this response, claims 1, 2, 10, 15, and 20 have been amended. Entry of the amendments to claims 1, 2, 10, 15, and 20 is respectfully requested. Reconsideration of the outstanding objections/rejections in the present application is also respectfully requested based on the following remarks.

At the outset, Applicant notes with appreciation the indication on page 4 of the Office Action that claims 18 and 19 are allowed. Applicant notes with equal appreciation the indication on page 4 of the Office Action that claims 11-14, 16, and 17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicant has opted to defer rewriting the above-identified claims in independent form pending reconsideration of the arguments presented below with respect to the rejected independent claims.

I. THE INFORMATION DISCLOSURE STATEMENT

On page 2 of the Office Action, the Examiner indicated that the information disclosure statement filed January 16, 2001, was

received but not considered because copies of the references cited therein were not provided.

As set forth in the information disclosure statement filed January 16, 2001, and in accordance with 37 CFR § 1.98(d), copies of the cited references were not previously provided because the same references were cited in prior U.S. Patent Application No. 09/372,319, filed August 11, 1999, now U.S. Patent No. 6,775,328, issued August 4, 2004. Accordingly, Applicant respectfully requests that the Examiner consider the references cited in the information disclosure statement filed January 16, 2001, and return an initialed PTO-1449 form to the undersigned indicating same.

II. THE OBJECTION TO THE DRAWINGS

On pages 2-3 of the Office Action, the drawings were objected to under 37 CFR § 1.83(a) for failing to every feature of the invention specified in the claims. This objection is hereby respectfully traversed with amendment.

The Examiner asserts that a master circuit comprising a slave circuit must be shown or the feature must be cancelled from claim 1. Applicant respectfully submits that claim 1 does not recite a master circuit comprising a slave circuit. Rather,

claim 1 recites a processing circuit having a slave circuit. Claim 1 has been amended to make this relationship more clear.

The Examiner also asserts that a second data output connected to the first data input must be shown or the feature must be cancelled from claim 20. Applicant respectfully submits that Figure 1 shows a second data output (output of driver 270) connected to the first data input (input of receiver 234). Claim 20 has been amended to make this relationship more clear.

In view of the foregoing, it is respectfully requested that the aforementioned objection to the drawings be withdrawn.

III. THE INDEFINITENESS REJECTION OF CLAIMS 1-9 AND 20

On page 3 of the Office Action, claims 1-9 and 20 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. This rejection is hereby respectfully traversed with amendment.

The Examiner asserts that, regarding claim 1, a master circuit comprising a slave circuit is not described in the specification and figures. Applicant respectfully submits that claim 1 does not recite a master circuit comprising a slave circuit. Rather, claim 1 recites a processing circuit having a

slave circuit. Claim 1 has been amended to make this relationship more clear.

The Examiner also asserts that, regarding claim 20, a second data output connected to the first data input is not described in the specification and figures. Applicant respectfully submits that Figure 1 shows a second data output (output of driver 270) connected to the first data input (input of receiver 234). Claim 20 has been amended to make this relationship more clear.

In view of the foregoing, it is respectfully requested that the aforementioned indefiniteness rejection of claims 1-9 and 20 be withdrawn.

IV. THE ANTICIPATION REJECTION OF CLAIMS 1, 2, 10, 15, AND 20

On page 4 of the Office Action, claims 1, 2, 10, 15, and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Dickerson et al. (U.S. Patent No. 4,617,423). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and

every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

The Examiner asserts that Dickerson et al. discloses the claimed invention. However, it is respectfully submitted that Dickerson et al. fails to disclose, with respect to claim 1, a communication device comprising a physical layer device and a processing circuit, wherein the physical layer device comprises a media driver connectable to a transmission medium, a media receiver connectable to the transmission medium, a serializer/deserializer (serdes) connected to the media driver and the media receiver, and a master circuit connected to the serdes, wherein the master circuit comprises a first physical layer data driver that drives a first differential signal, and a first physical layer data receiver, and wherein the processing

circuit comprises an internal circuit and a slave circuit connected to the internal circuit and the master circuit, wherein the slave circuit comprises a first processing data receiver connected to the first physical layer data driver that outputs a first signal in response to receiving the signal output from the first physical layer data driver, and a first processing data driver connected to the first physical layer data receiver and connectable to the first processing data receiver. Specifically, the Examiner fails to describe how Dickerson et al. discloses, or even suggests, the claim elements of: 1.) a physical layer device; 2.) a processing circuit; 3.) a physical layer device comprising a media driver connectable to a transmission medium; 4.) a physical layer device comprising a media receiver connectable to the transmission medium; 5.) a physical layer device comprising a serializer/deserializer (serdes) connected to the media driver and the media receiver; 6.) a physical layer device comprising a master circuit connected to the serdes; 7.) a master circuit comprising a first physical layer data driver that drives a first differential signal; 8.) a master circuit comprising a first physical layer data receiver; 9.) a processing circuit comprising an internal circuit; 10.) a processing circuit comprising a slave circuit connected to the internal circuit and the master circuit; 11.) a

slave circuit comprising a first processing data receiver connected to the first physical layer data driver that outputs a first signal in response to receiving the signal output from the first physical layer data driver; and 12.) a slave circuit comprising a first processing data driver connected to the first physical layer data receiver and connectable to the first processing data receiver. As stated in MPEP § 2131, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Accordingly, it is respectfully submitted that Dickerson et al.

fails to disclose, or even suggest, the limitations as recited in claim 1.

It is also respectfully submitted that Dickerson et al. fails to disclose, with respect to claim 10, a processing circuit, comprising an internal circuit and a slave circuit connected to the internal circuit, wherein the slave circuit comprises a clock receiver connectable to a clock driver that outputs a clock signal in response to a first differential signal received from the clock driver, a first processing data receiver connectable to the first physical layer data driver that outputs a first signal in response to a second differential signal received from the first physical layer data driver, and a first processing data driver connectable to a first physical layer data receiver to receive the clock signal from the clock receiver or the first signal from the first processing data receiver. Specifically, the Examiner fails to describe how Dickerson et al. discloses, or even suggests, the claim elements of: 1.) an internal circuit; 2.) a slave circuit connected to the internal circuit; 3.) a slave circuit comprising a clock receiver connectable to a clock driver that outputs a clock signal in response to a first differential signal received from the clock driver; 4.) a slave circuit comprising a first processing data receiver connectable to the first physical layer

data driver that outputs a first signal in response to a second differential signal received from the first physical layer data driver; and 5.) a slave circuit comprising a first processing data driver connectable to a first physical layer data receiver to receive the clock signal from the clock receiver or the first signal from the first processing data receiver. As stated in MPEP § 2131, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Accordingly, it is respectfully submitted that Dickerson et al. fails to disclose, or even suggest, the limitations as recited in claim 10.

It is further respectfully submitted that Dickerson et al. fails to disclose, with respect to claim 15, a physical layer device connectable to a transmission medium comprising a media driver connectable to the transmission medium, a media receiver connectable to the transmission medium, a serializer/deserializer (serdes) connected to the media driver and the media receiver, wherein the serdes outputs a master clock signal, an equivalent in-phase slave clock signal when in a calibration mode, and a data signal when in a data mode, wherein the data signal represents a data signal received from the media receiver, and a master circuit comprising a clock driver connected to output the master clock signal as a first differential signal, and a first physical layer data driver connectable to output the slave clock signal as a second differential signal when the serdes is in the calibration mode, and the data signal as a third differential signal when the serdes is in the data mode. Specifically, the Examiner fails to describe how Dickerson et al. discloses, or even suggests, the claim elements of: 1.) a media driver connectable to a transmission medium; 2.) a media receiver connectable to the transmission medium; 3.) a serializer/deserializer (serdes) connected to the media driver and the media receiver, wherein the serdes outputs a master clock signal, an equivalent in-phase

slave clock signal when in a calibration mode, and a data signal when in a data mode, wherein the data signal represents a data signal received from the media receiver; and 4.) a master circuit comprising a clock driver connected to output the master clock signal as a first differential signal, and a first physical layer data driver connectable to output the slave clock signal as a second differential signal when the serdes is in the calibration mode, and the data signal as a third differential signal when the serdes is in the data mode. As stated in MPEP § 2131, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d

1955, 1957 (Fed. Cir. 1993). Accordingly, it is respectfully submitted that Dickerson et al. fails to disclose, or even suggest, the limitations as recited in claim 15.

It is still further respectfully submitted that Dickerson et al. fails to disclose, with respect to claim 20, a communication device comprising a physical layer device and a processing circuit, wherein the physical layer device is connectable to a transmission medium and comprises a master circuit comprising a clock output, a first data output, a first data input, and a phase comparator connected to the first data input, and wherein the processing circuit comprises a slave circuit comprising a clock input connected to the clock output, a second data input connected to the first data output, a second data output connected to the first data input, and a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output, wherein the phase comparator compares a phase of the output signal from the clock input with a phase of the output signal from the second data input to determine a phase difference. Specifically, the Examiner fails to describe how Dickerson et al. discloses, or even suggests, the claim elements of: 1.) a physical layer device connectable to a transmission medium and comprising a master circuit; 2.) a

master circuit comprising a clock output, a first data output, a first data input, and a phase comparator connected to the first data input; 3.) a processing circuit comprising a slave circuit; 4.) a slave circuit comprising a clock input connected to the clock output, a second data input connected to the first data output, a second data output connected to the first data input, and a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output; and 5.) the phase comparator comparing a phase of the output signal from the clock input with a phase of the output signal from the second data input to determine a phase difference. As stated in MPEP § 2131, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or

characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Accordingly, it is respectfully submitted that Dickerson et al. fails to disclose, or even suggest, the limitations as recited in claim 20.

Claim 2 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 2 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, claim 2 recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, it is respectfully submitted that Dickerson et al. fails to disclose, with respect to claim 2, a master circuit comprising a clock driver connected to a serdes for driving a second differential signal, a slave circuit comprising a clock receiver connected to the clock driver for outputting a clock signal in response to a signal received from the clock driver, and a first processing data driver connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver, wherein a first physical layer data receiver receives the clock signal when the first processing data driver is connected to receive the clock

signal, and the first signal when the first processing data driver is connected to receive the first signal.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 10, 15, and 20 be withdrawn.

V. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

TEA/vrp

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

Date: September 29, 2004

APPENDIX A

1 (Currently Amended). A communication device comprising:

a physical layer device having:

a media driver connectable to a transmission medium;

a media receiver connectable to the transmission medium; ~~and~~

a serializer/deserializer (serdes) connected to the media driver and the media receiver; and

a master circuit connected to the serdes, the master circuit having:

a first physical layer data driver, the first physical layer data driver driving a ~~millivolt~~ first differential signal; and

a first physical layer data receiver; and

a processing circuit having:

an internal circuit; and

a slave circuit connected to the internal circuit and the master circuit, the slave circuit having:

a first processing data receiver connected to the first physical layer data driver, the first processing data receiver outputting a first signal in response to receiving the signal output from the first physical layer data driver; and

a first processing data driver connected to the

first physical layer data receiver, and connectable to the first processing data receiver.

2 (Currently Amended). The device of Claim 1,

wherein the master circuit further includes a clock driver connected to the serdes, the clock driver driving a ~~millivolt~~ second differential signal;

wherein the slave circuit further includes a clock receiver connected to the clock driver, the clock receiver outputting a clock signal in response to a signal received from the clock driver; and

wherein the first processing data driver is connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver, the first physical layer data receiver receiving the clock signal when the first processing data driver is connected to receive the clock signal, and the first signal when the first processing data driver is connected to receive the first signal.

3 (Original). The device of claim 2 wherein the master circuit further comprises an aligner connected to the first physical layer data receiver, the aligner receiving the clock signal when the first physical layer data receiver receives the clock

signal, the aligner receiving the first signal when the first physical layer data receiver receives the first signal, the aligner having phase comparison circuitry that compares a phase of the clock signal received by the aligner with a phase of the first signal received by the aligner to determine a phase difference.

4 (Original). The device of claim 3 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signal to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the signal output from the first physical layer data driver so that the first signal received by the aligner is substantially in phase with the clock signal received by the aligner.

5 (Original). The device of claim 4 wherein the slave circuit further includes:

a first multiplexor connected to the clock input receiver and the first processing data receiver, the first multiplexor passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the

first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexor connected to the first multiplexor and the first communication data driver, the second multiplexor passing a signal output from the first multiplexor when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexor being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

6 (Original). The device of claim 5 wherein the slave circuit further includes a serial-to-parallel shift register connected to the clock receiver, the first processing data receiver, and the internal circuit, the clock signal output by the clock receiver clocking the shift register.

7 (Original). The device of claim 5 wherein the slave circuit further includes a parallel-to-serial shift register connected to the internal circuit, the second multiplexor, and the clock receiver, the shift register outputting a data output signal in response to a parallel data signal from the internal circuit,

the clock signal output by the clock receiver clocking the parallel-to-serial shift register.

8 (Original). The device of claim 7 wherein the slave circuit further includes a logic circuit connected to the first mux, the second mux, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

9 (Original). The device of claim 8 wherein the media receiver receives a signal from the transmission media having a first frequency, wherein the signal output from the serdes has a second frequency, and wherein the first frequency and the second frequency are substantially equivalent.

10 (Currently Amended). A processing circuit comprising:

an internal circuit; and

a slave circuit connected to the internal circuit, the slave circuit having:

a clock receiver connectable to a clock driver, the clock receiver outputting a clock signal in response to a first

~~millivolt~~ differential signal received from the clock driver;

a first processing data receiver connectable to the first physical layer data driver, the first processing data receiver outputting a first signal in response to a second ~~millivolt~~ differential signal received from the first physical layer data driver; and

a first processing data driver connectable to a first physical layer data receiver, the first processing data driver being connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver.

11 (Original). The circuit of claim 10 wherein the slave circuit further comprises:

a first multiplexor connected to the clock input receiver and the first processing data receiver, the first multiplexor passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexor connected to the first multiplexor and the first communication data driver, the second multiplexor passing a signal output from the first multiplexor when a second

mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexor being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

12 (Original). The circuit of claim 11 wherein the slave circuit further comprises a serial-to-parallel shift register connected to the internal circuit, the clock receiver, and the first processing data receiver, the clock signal output by the clock receiver clocking the shift register.

13 (Original). The circuit of claim 12 wherein the slave circuit further comprises a parallel-to-serial shift register connected to the internal circuit, the second multiplexor, and the clock receiver, the parallel-to-serial shift register outputting a data output signal in response to a parallel data signal from the internal circuit, the clock signal output by the receiver clocking the parallel-to-serial shift register.

14 (Original). The circuit of claim 13 wherein the slave circuit further includes a logic circuit connected to the first mux, the

second mux, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

15 (Currently Amended). A physical layer device connectable to a transmission medium, the device comprising:

a media driver connectable to the transmission medium;

a media receiver connectable to the transmission medium;

a serializer/deserializer (serdes) connected to the media driver and the media receiver, the serdes outputting a master clock signal, an equivalent in-phase slave clock signal when in a calibration mode, and a data signal when in a data mode, the data signal representing a data signal received from the media receiver; and

a master circuit, the master circuit having:

a clock driver connected to output the master clock signal as a first ~~millivolt~~ differential signal; and

a first physical layer data driver connectable to output the slave clock signal as a second ~~millivolt~~ differential signal when the serdes is in the calibration mode, and the data signal as a third ~~millivolt~~ differential signal when the serdes

is in the data mode.

16 (Original). The device of claim 15 wherein the master circuit further includes:

a first physical layer data receiver that receives a signal which represents the master clock signal during a first phase of the calibration mode, and represents the slave clock signal during a second phase of the calibration mode; and

an aligner connected to the first physical layer data receiver, the aligner receiving the master clock signal when the first physical layer data receiver receives the master clock signal, and the slave clock signal when the first physical layer data receiver receives the slave clock signal, the aligner having phase comparison circuitry that compares a phase of the master clock signal received by the aligner with a phase of the slave clock signal received by the aligner to determine a phase difference.

17 (Original). The device of claim 16 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signals to the phase delay circuit that indicates the phase difference, the phase delay

circuit delaying the slave clock signal output from the serdes an amount so that the slave clock signal received by the aligner is substantially in phase with the master clock signal received by the aligner when in the calibration mode, the data signal being delayed the amount when in the data mode.

18 (Original). A method for operating a communication device having a physical layer device connected to a transmission medium and a processing device connected to the physical layer device, the method comprising the steps of:

outputting a master clock signal from the physical layer device over a first path;

receiving the master clock signal in the processing device from the first path;

outputting the master clock signal as a feedback master clock signal from the processing device over a feedback path;

receiving the feedback master clock signal in the physical layer device from the feedback path;

determining a phase of the feedback master clock signal;

outputting a slave clock signal from the physical layer device over a second path after the phase of the feedback master clock signal has been determined, the master clock signal and the slave clock signal having an equivalent frequency;

receiving the slave clock signal in the processing device from the second path;

outputting the slave clock signal as a feedback slave clock signal from the processing device over the feedback path;

receiving the feedback slave clock signal in the physical layer device from the feedback path;

determining a phase of the feedback slave clock signal;

comparing the phase of the feedback master clock signal with the phase of the feedback slave clock signal to determine a phase difference; and

adjusting a delay so that the phase of the feedback slave clock signal is substantially aligned with the phase of the feedback master clock signal.

19 (Original). The method of claim 18 and further comprising the steps of:

outputting a data clock signal from the physical layer device over the first path after the phase difference has been determined;

outputting an input data signal from the physical layer device over the second path after the phase difference has been determined, the input data signal and data clock signal having an equivalent frequency; and

converting the input data signal to a parallel word by clocking the input data signal with the data clock signal.

20 (Currently Amended). A communication device comprising:

a physical layer device connectable to a transmission medium, the device having a master circuit, the master circuit having:

a clock output;

a first data output;

a first data input; and

a phase comparator connected to the first data input; and

a processing circuit having a slave circuit, the slave circuit having:

a clock input connected to the clock output;

a second data input connected to the first data output ~~input~~;

a second data output connected to the first data input; and

a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output, the phase comparator comparing a phase of the output signal from the clock

input with a phase of the output signal from the second data input to determine a phase difference.